Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **Regulated Output (Power)**
2. **Regulated Output (Measure)**
3. **GND**
4. **Unregulated Input**

**.066”**

**3**

**2**

**1**

**4**

**.092”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004 x .004”**

**Backside Potential: VCC**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .066” X .092” DATE: 4/2/21**

**MFG: SGS THICKNESS .015” P/N: 7805**

**DG 10.1.2**

#### Rev B, 7/1